REMARKS

This is in response to the Office Action dated April 1, 2004. Claims 6 and 10 have been canceled. Thus, claims 1, 4-5, 7-9, 11 and 24 are now pending.

Drawing Objections

The drawings stand objected to in paragraph 2 of the Office Action. This drawing objection is respectfully traversed for at least the following reasons. Figs. 1(a) and 1(b) clearly illustrates NMOS and PMOS types of transistors (e.g., first and second MOS transistors of different conductivity types). The specification clearly explains that features at issue apply to both types of transistor (e.g., pg. 12, line 14 to pg. 15, line 24). Fig. 3(a) is an example of a NMOS transistor in this regard. Both NMOS and CMOS transistors with corresponding wells 31a, 31b, 31c are illustrated in Figs. 4(a)-(d), and element isolation regions 37 in such transistors are shown in Figs. 4 and 5. Furthermore, Fig. 8 also illustrates contacts 50 formed in the trench isolation regions 46 (e.g., see pg. 29, lines 7-10). Clearly, the drawings are much more than sufficient in this regard.

Formality Objections

The claims stand objected to in paragraph 3 of the Office Action for formality reasons. It is respectfully submitted that the claim amendments herein address and overcome any potential issue in this regard. In particular, (a) claims 1, 7 and 24 have been amended by inserting "and in" after "on" at line 2; (b) claim 1, line 23, has been amended by deleting "separate of"; (c) claims 6 and 10 recite "substantially" electrically isolated thereby taking into account separation by only the substrate – this is entirely

proper; and (d) claim 10 has been canceled and certain subject matter thereof has been added to claim 7. Thus, the formality objections in paragraph 3 have been addressed and overcome.

Section 112 Rejection

Claim 1 stands rejected under 35 U.S.C. Section 112, first paragraph, in paragraph 4 of the Office Action. This Section 112 rejection is respectfully traversed for at least the following reasons.

A transistor being "substantially completely depleted" means that a depletion layer on the gate electrode side and a depletion layer on the semiconductor layer surface side are connected to each other. In the case of an NMOS transistor for example, "substantially completely depleted in the standby state" means that the transistor is in an OFF state at a gate voltage of 0 V for example and the depletion layers are connected to each other. The transistors being "substantially completely depleted" in the operative state means, in the case of an NMOS transistor for example, that the transistor is in an ON state by application of a given voltage (e.g., positive voltage) and the depletion layers are connected to each other. By making the transistors "substantially completely depleted" in the operative state, the parasitic capacitance can be advantageously reduced thereby permitting a higher speed of operation to be achieved.

Furthermore, the transistor may change the threshold voltage depending upon the standby/operative state. In other words, when the transistor is in the standby state, its threshold is changed to prevent (or reduce) a current from flowing in the transistor; that

is, to reduce an OFF current. When the transistor is of the NMOS type for example, a bias voltage is applied to the well on the substrate side so that the threshold is increased.

When the transistor is in the operative state, its threshold is changed to help a current to easily flow in the transistor; that is, to allow for a high speed operation of the transistor. When the transistor is of the NMOS type, a bias voltage is set so as to lower the threshold.

In the Office Action, the Examiner asked - - how can the active regions of the first and second transistors be substantially completely depleted simultaneously in the standby state. In this regard, the transistor structure has an NMOS transistor and a PMOS transistor respectively formed in independent wells, and therefore, a bias voltage can be applied separately to each well. This allows the two transistors to be substantially completely depleted simultaneously in the standby state. This is supported by the instant specification, for example, at page 24, lines 9-25.

In the Office Action, the Examiner also asked - - how can the on-state transistor also have a depleted active region. In this regard, for example, since the CMOS transistor has NMOS and PMOS transistors respectively formed in the independent wells as described above, it is possible to have both transistors simultaneously in the standby state.